Features

- **50K Rads(Si) Min. TID**
- **Latch-up Immune up to 85 MeV cm²/mg LET**
- **Crystal Mounted at 4 Points**
- **High Shock & Vibration Design**
- **Tristate Enable/Disable function is provided by default**
- Low Profile Surface Mount Package
- 100% Screening per MIL-PRF-55310 Level B plus PIND
- Low Phase Noise
- Hermetically Sealed, Ceramic Package
- Tape & Reel packaging
- Made in USA, ECCN: EAR99

Applications

- New Space, LEO
- Micro & Nano Satellites
- Commercial Satellites

Package Specifications & Outline:

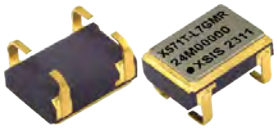
- Package: Ceramic 90% AL_2O_3
- Seal: Hermetic – Resistance Welded
- Weight: 0.15g typical, 0.2g Max.
- Thermal Resistance, Junction to Case (θ_{JC}): 38 °C / Watt
- Solder Reflow Temp./Time: 260 °C Max for 10 Seconds Max.
- Pad Finish: 1.27 to 1.9 µm gold over 2.0 to 3.5 µm nickel
- Lead Material & Finish: Kovar, 40 to 70 µ inches gold
  Over 100 to 250 µ inches Nickel

Hot Solder Tinning per MIL-PRF-55310 is optional at additional cost.

Contact Xsis Electronics at xsis@xsis.com for any special requirements.

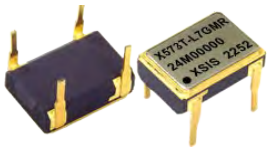
Package Options

"X57T"



"X571T"

"X572T"



"X573T"

ORDERING INFORMATION (Please build your part number from options below) :

P/N EXAMPLE: X57T- L7MR- 24.000 MHz = **3.3V HCACMOS, ± 75 PPM Overall Frequency Accuracy over -55 °C to +125 °C, Tristate Output , 100% Screening, Swept Quartz Crystal, 24.000 MHz**

X57T – **L** **7** **M** **R** – Output Frequency

Package Options
See Page 7

Swept Quartz Options
Add **"R"** if Swept Quartz is required

100% Screening Options

X =	No Screening, Engineering Model
M =	Screening per MIL-PRF-55310 Level B + PIND

Supply Voltage & Output Type

A =	5.0V, HC/ACMOS
L =	3.3V, LVHCMOS
N =	2.5V, LVHCMOS
R =	1.8V, LVHCMOS

*** Overall Frequency Accuracy Options**

1 =	± 50 PPM	over -10 °C	to	+70 °C
2 =	± 25 PPM	over -10 °C	to	+70 °C
3 =	± 100 PPM	over -40 °C	to	+85 °C
4 =	± 50 PPM	over -40 °C	to	+85 °C
5 =	± 25 PPM	over -40 °C	to	+85 °C
6 =	± 100 PPM	over -55 °C	to	+125 °C
7 =	± 75 PPM	over -55 °C	to	+125 °C
8 =	± 60 PPM	over -55 °C	to	+125 °C
9 =	± 50 PPM	over -55 °C	to	+105 °C

*Overall frequency accuracy includes: initial accuracy, frequency changes due to temperature, supply voltage, load variations and **5 year aging**.

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Table I - Electrical Specifications, 5V HC/ACMOS/TTL & 3.3V LVHCMOS Oscillators

Parameter	5V	3.3V
Output Frequency Range	500 KHz to 105 MHz	500 KHz to 160 MHz
Overall Frequency Accuracy ***(See Note Below)***	See Options in the Ordering Information on Page 1	
Operating Temperature Range	See Options in the Ordering Information on Page 1	
Supply Voltage (Vdd)	+ 5.0V ± 10%	3.3V ± 10%
Input Current (no Load)	500 KHz - 8 MHz 4 mA Max. 8.1 MHz - 32 MHz 10 mA Max. 32.1 MHz - 64 MHz 40 mA Max. 64.1 MHz - 105 MHz 60 mA Max.	500 KHz - 8 MHz 3 mA Max. 8.1 MHz - 32 MHz 6 mA Max. 32.1 MHz - 64 MHz 25 mA Max. 64.1 MHz - 100 MHz 40 mA Max. 100.1 MHz - 130 MHz 50 mA Max. 130.1 MHz - 160 MHz 60 mA Max
Output Waveform	Square Wave, HC/ACMOS/TTL Compatible	Square Wave, LVHCMOS Compatible
Output Duty Cycle – TTL (at 1.4V Output Level)	60/40% Max.	N/A
Output Duty Cycle – HCMOS (at 50% Level)	45/55%	
Output High Level	0.9 Vdd Min.	0.9 Vdd Min.
Output Low Level	0.1 Vdd Max.	0.1 Vdd Max.
Output Current	± 16 mA Max.	± 8 mA Max.
Output Load	10K // 15 pF or 8TTL loads Max. 50 pF Max. ≤ 50 MHz 30 pF Max. > 50 MHz	10K // 15 pF 30 pF Max. ≤ 50 MHz
Rise & Fall Times (Typical Load) (at 10% to 90% Output Levels)	≤ 40 MHz 6 nS Max. 40 MHz to 75 MHz 3 nS Max. > 75 MHz 2 nS Max.	≤ 40 MHz 6 nS Max. 40 MHz to 75 MHz 3 nS Max. > 75 MHz 2 nS Max.
Tristate Input	≥ 3.5V or Open : Normal Output ≤ 0.8V: High Impedance	≥ 0.7 Vdd or Open : Normal Output ≤ 0.3 Vdd: High Impedance
Start-Up Time	10 mS Max.	10 mS Max.
Phase Jitter (10 KHz - 20 MHz Integrated)	0.3 pS rms Typical	0.3 pS rms Typical
Aging at 70 °C	± 3 PPM Max. first year, ± 2 PPM Max. per year thereafter	
Absolute Maximum Applied Voltage	+ 7 VDC	+ 5 VDC
Storage Temperature	-65 °C to +125 °C	-65 °C to +125 °C

NOTE: Overall Frequency Accuracy Includes, Initial Accuracy at 25 °C, Frequency changes over Operating Temperature, Aging over 5 years, Frequency changes due to Supply Voltage & Load Variations.

For special requirements, please contact Xsis Electronics at xsis@xsis.com or call us at 913-631-0448.

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Table II - Electrical Specifications, 2.5V & 1.8V LVHCMOS Oscillators

Parameter	2.5V " Model X57T-N "	1.8V " Model X57T-R "
Output Frequency Range	500 KHz to 135 MHz	500 KHz to 125 MHz
Overall Frequency Accuracy ***(See Note Below)***	See Options in the Ordering Information on Page 1	
Operating Temperature Range	See Options in the Ordering Information on Page 1	
Supply Voltage (Vdd)	2.5V ± 10%	1.8V ± 10%
Input Current (no Load)	500 KHz-8 MHz 3 mA Max. 8.1 MHz-16 MHz 4 mA Max. 16.1 MHz-32 MHz 8 mA Max. 32.1 MHz-60 MHz 15 mA Max. 60.1 MHz-100 MHz 20 mA Max. 100.1 MHz-135 MHz 30 mA Max.	500 KHz-8 MHz 3 mA Max. 8.1 MHz-16 MHz 4 mA Max. 16.1 MHz-32 MHz 6 mA Max. 32.1 MHz-60 MHz 10 mA Max. 60.1 MHz-85 MHz 20 mA Max. 85.1 MHz-125 MHz 25 mA Max.
Output Waveform	Square Wave, LVHCMOS Compatible	
Output Duty Cycle (at 50% Output Level)	45/55%	
Output High Level	0.9 Vdd Min.	
Output Low Level	0.1 Vdd Max.	
Output Current	± 4 mA Max	
Output Load	10K // 15 pF	
Rise & Fall Times (Typical Load) (at 10% to 90% Output Levels)	≤ 40 MHz 6 nS Max. 40 MHz to 75 MHz 3 nS Max. > 75 MHz 2 nS Max.	≤ 40 MHz 6 nS Max. 40 MHz to 75 MHz 3 nS Max. > 75 MHz 2 nS Max.
Tristate Input	≥ 0.7 Vdd or Open : Normal Output ≤ 0.3 Vdd: High Impedance	
Start-Up Time	10 mS Max.	
Phase Jitter (10 KHz - 20 MHz Integrated)	0.3 pS rms Typical	0.3 pS rms Typical
Aging at 70 °C	± 3 PPM Max. first year, ± 2 PPM Max. per year thereafter	
Absolute Maximum Applied Voltage	+ 4.5 VDC	
Storage Temperature	-65 °C to +125 °C	

NOTE: Overall Frequency Accuracy Includes, Initial Accuracy at 25 °C, Frequency changes over Operating Temperature, Frequency changes due to Supply Voltage & Load Variations and Aging over 5 years

For special requirements, please contact Xsis Electronics at xsis@xsis.com or call us at 913-631-0448.

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Table III - 100% Screening per MIL-PRF-55310 Level B, Including PIND

Test - Inspection	Test Method – Condition
Internal Visual	MIL-STD-883, Method 2017, Level B
Stabilization Bake (Prior to Seal) 1/	MIL-STD-883, Method 1008, Condition C, (+150 °C), 24 hours minimum
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Constant Acceleration	MIL-STD-883, Method 2001, Condition A, Y_1 axis only (5000 G)
Seal (Fine and Gross Leak)	MIL-PRF-55310, Para. 4.8.2.2.2 ($1(10)^{-8}$ atm-cc/s Max.)
Particle Impact Noise Detection (PIND)	MIL-STD-883, Method 2020, Condition A
Pre Burn-in Electrical Tests: Record as applicable	Refer to Table III-a below
Burn-in	+125 °C, Nominal Supply Voltage and Burn-in load, 160 Hours Minimum
Post Burn-in Electrical Tests: Record as applicable	Refer to Table III-a below
External Visual	MIL-STD-883, Method 2009

1/ Vacuum bake and maintain oscillators in dry nitrogen per MIL-PRF-55310

Table III-a – Pre & Post Burn-in Electrical Tests

Test Parameter	MIL-PRF-55310 Method	Pre BI 24 ± 1 °C	Post BI 24 ± 1 °C	Post BI Low Temp	Post BI High Temp
Input Current	4.8.5	✓	✓	✓	✓
Output Frequency	4.8.6	✓	✓	✓	✓
Frequency Vs. Temperature Stability	4.8.10.1		✓	✓	✓
Frequency Vs. Supply Voltage	4.8.14		✓	✓	✓
Output Voltage Levels	4.8.21.3	✓	✓	✓	✓
Output Rise & Fall Times	4.8.22	✓	✓	✓	✓
Output Duty Cycle	4.8.23	✓	✓	✓	✓
Start-up time	4.8.29		✓	✓	✓
Tristate, if applicable	4.8.28		✓	✓	✓

Quality Conformance Inspection: Group A per MIL-PRF-55310, Level B

Following QCI Options are available at additional cost:

Group B per MIL-PRF-55310, Level B
Non-distruct Bond Pull per MIL-STD-883, Method 2023
Radiographic Inspection per MIL-STD-883. Method 2012, Class S
DPA (Destructive Physical Analysis) per Customer Specified Method
Life Test per MIL-STD-883, Method 105, 1000 Hrs. at +125 °C

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Packaging: Tape & Reel, See Page 6

Thermal Characteristics:

Junction to case Thermal Constant (θ_{JC}): 38 °C / Watt
Junction to Ambient (Device floating in free air) Thermal Constant (θ_{JA}): 135 °C / Watt

Table IV - TID and SEE Tolerances:

TID	SEL	SET/SEU	SEFI
50Krads (Si) Min.	75 MeV cm²/mg Min. at 125°C	24 MeV cm²/mg Min.	75 MeV cm²/mg Min.

Table V - Typical Phase Noise (dbc/Hz):

Output Frequency	10 Hz	100 Hz	1 KHz	10 KHz	100 KHz	1 MHz
10 MHz	- 90	-122	-145	-158	-161	-164
25 MHz	-83	-111	-140	-148	-155	-157
50 MHz	-81	-108	-133	-142	-146	-154
96 MHz	-79	-106	-132	-141	-147	-153
110 MHz	-77	-106	-131	-140	-146	-153

Table VI - Environmental Specifications:

X57xT series oscillators are designed to meet or exceed the Environmental tests specified below. Customized screening and environmental testing are also available to meet your special requirements.

Test	Test Conditions
Vibration	0.06" DA, 30 G peak, 10 - 2000 Hz, MIL-STD-202, Method 204, Cond. G
Shock	5000 G, 0.5 mS, half-Sine, MIL-STD-883, Method 2002, Cond. B modified
Temperature Cycling	MIL-STD-883, Method 1010, Cond. C
Thermal Shock	MIL-STD-202, Method 107, Cond. B
Seal (Fine and Gross)	MIL-STD-883, Method 1014 Cond. A & C
Burn-in	160 Hours, 125 °C, Nominal Supply Voltage & Load
Frequency Aging	± 1.5 PPM Max. first 30 days, ± 3 PPM Max. first year, ± 2 PPM Max. per year thereafter
Altitude	MIL-STD-202, Method 105, Cond. C
Constant Acceleration	MIL-STD-883, Method 2001, 5000 G
Moisture Resistance	MIL-STD-202, Method 106, Vibration Sub Cycle Omitted
Solderability	MIL-STD-202, Method 208
Resistance to Soldering Heat	MIL-STD-202, Method 210, Cond B. or C as applicable
Resistance to Solvents	MIL-STD-202, Method 215
Internal Water Vapor Content	MIL-STD-883, Method 1018
ESD Classification	MIL-STD-883, Method 3015, Class 1C, HBM 1000 to 1999
Moisture Sensitivity Level	J-STD-020, MSL=1

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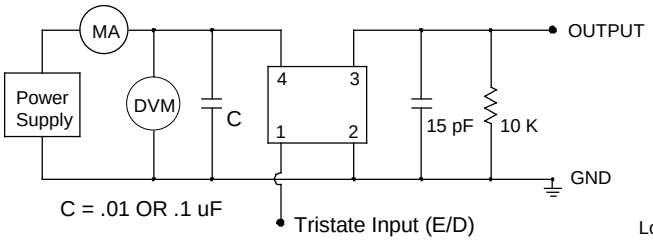
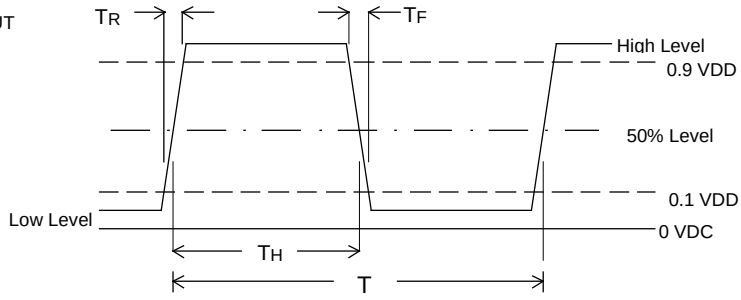
HCMOS Test Circuit



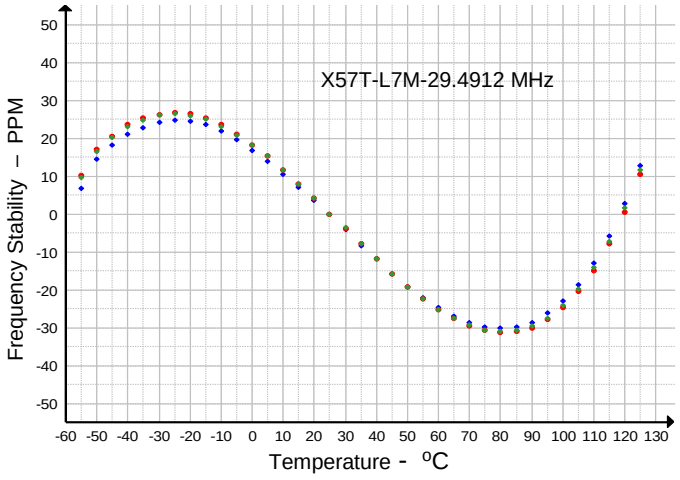
Tristate Input has an internal pull-up resistor. It can be left floating or connected to Vdd.

HCMOS Output Waveform

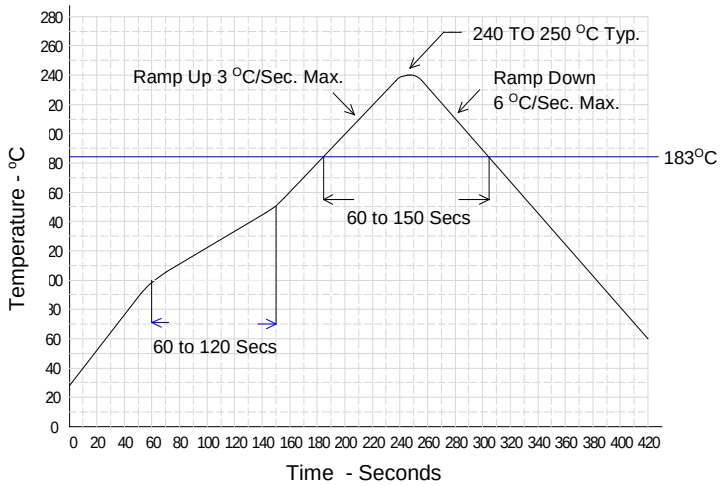


$$\text{Symmetry} = \frac{T_H}{T} \times 100\ \%$$

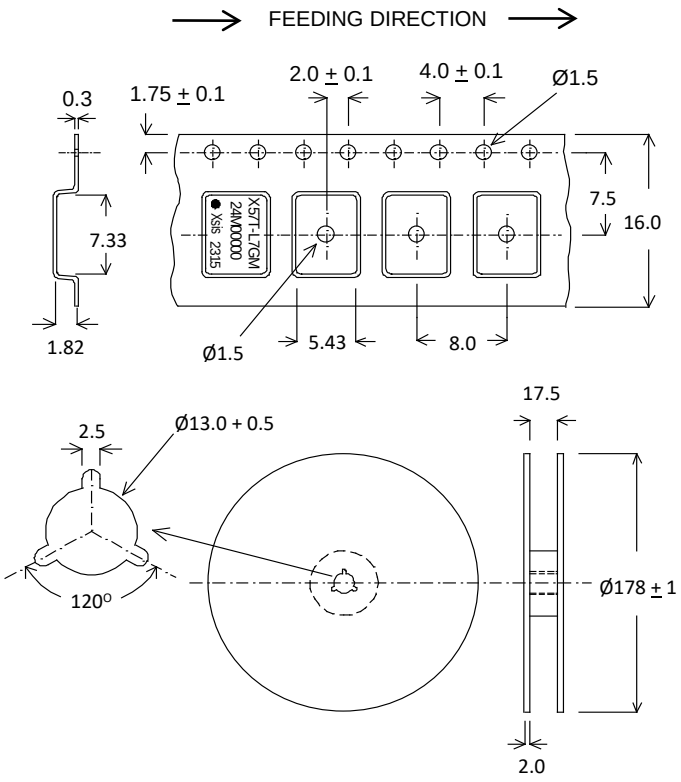
Typical Freq. Stability Vs. Temperature



Typical Solder Reflow Profile



Tape & Reel Data for X57T parts



Dimensions are in mm.

Tape is EIA-481-A Compliant.

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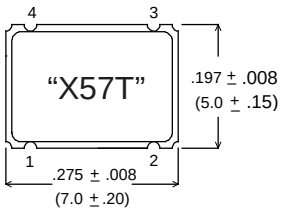
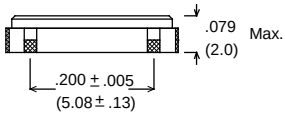
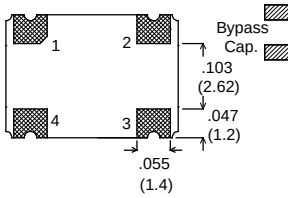
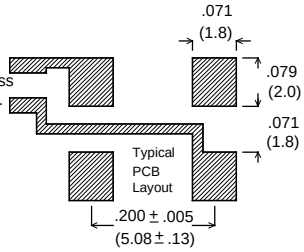
Package Outline and Pin Connections – Dimensions are in inches (mm)

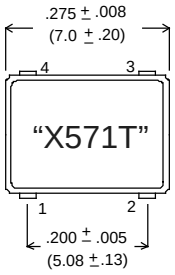


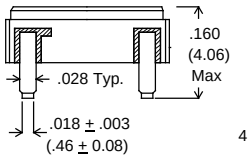
LEAD/PAD#	FUNCTION
1	ENABLE/DISABLE
2	GND/CASE
3	OUTPUT
4	VDD

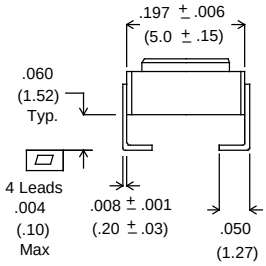


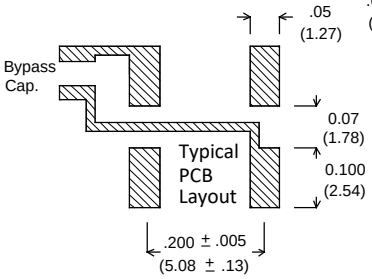








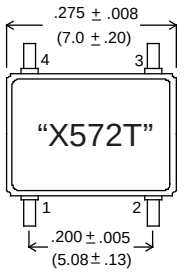


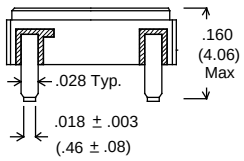


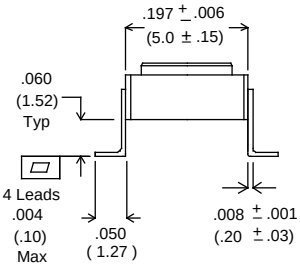
An External 0.01uF Bypass Capacitor is required between VDD and GND.

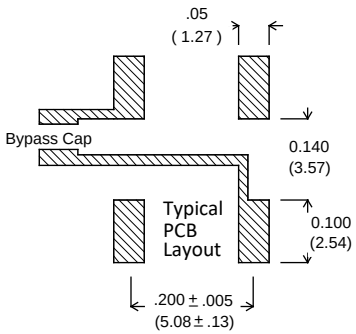
E/D (Enable/Disable) Input: A "Low" level at the input disables the Output into a high impedance state.

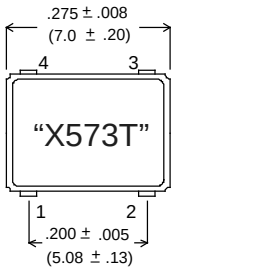
E/D Input has internal pull-up. It can be left floating or connected to Vdd.

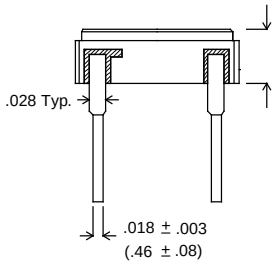


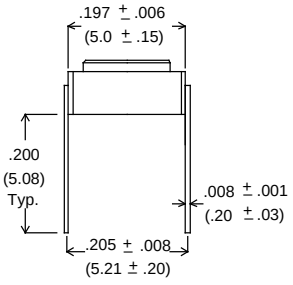


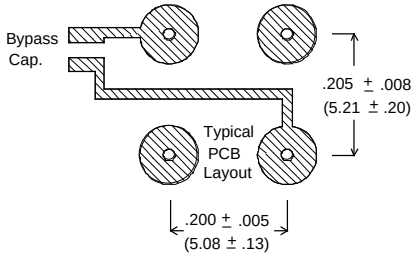












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